

## COPY OF PAPERS

Examiner:

Art Unit:

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE Or. TECHNOLOGIES TO THE CENTER 28"

In re Application of:

SOBEK, et al.

Serial No.: 09/885,426

Filed: June 19, 2001

A SILICIDED BURIED For:

> BITLINE PROCESS FOR A NON-VOLATILE MEMORY

CELL

Assistant Commissioner of Patents and Trademarks Washington, D.C. 20231

Dear Sir:

## RESPONSE TO RESTRICTION REQUIREMENT

In the Office Action mailed June 18, 2002, the Examiner has stated that the present Application contains claims directed to two distinct inventions, Invention I and Invention II. Specifically, the Examiner contends that the first invention, Invention I, is represented by Claims 1-13 and is drawn to a semiconductor device, classified in class 257, subclass 314. The Examiner further contends that the second invention, Invention II, is represented by Claims 14-30 and is drawn to process for making semiconductor devices, classified in class 438, subclass 22+. As such, the Examiner has required Applicants to elect an invention for prosecution on the merits.

Serial No.: 09/885,426 Group Art Unit: 2811

1